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A TECHNIQUE TO MEASURE THE DYNAMIC RESPONSE OF a-Si:H THIN FILM TRANSISTOR CIRCUITS

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INTRODUCTION

Hydrogenated amorphous silicon TFT logic circuits have become an important issue to several commercial display applications. It is highly desirable to fabricate the driver circuitry of the TFT switching matrix, in an active matrix LCD, with a-Si:H technology because of the reduction in cost and improvement in the reliability[1]. As the development in this technology progresses, it is becoming increasingly important to measure and characterize the dynamic response of a-Si:H or polysilicon TFT circuits, such as inverters and shift registers. The measurement is essential to confirm the modeling techniques and to determine the characteristic speed of operation of the circuit.

The output resistance of an a-Si:H TFT is very high. It can typically vary from $10^6\,\Omega$ in the ON state to $10^{12}\,\Omega$ in the OFF state[2]. Even the on state resistance could be larger than or at least comparable to the input impedance of the dynamic measurement instrument such as an oscilloscope. Thus, the scope cannot be placed in parallel with the output of the TFT, since this will change the loading characteristics of the circuit. To the author's knowledge, an instrument with input impedance greater than $10^{12}\,\Omega$ and the capability of performing dynamic measurement is not available.

It is the purpose of this note to present an indirect technique to measure the dynamic response of a-Si:H circuits. The measurement requires only a storage oscilloscope and a d.c. electrometer. The effect of charge trapping in the TFTs, as it relates to the measurement, is also discussed. The technique is applied to an enhancement-type a-Si:H TFT inverter circuit with a capacitor load and the results are presented.

TECHNIQUE

An a-Si:H enhancement load TFT inverter is shown in Fig. 1. The output voltage to be obtained is across the capacitor C_L. In the proposed technique, a small resistor is placed in series with the load capacitor and the voltage across the resistor, V_R, is measured by a digitizing oscilloscope. The output voltage is then given by

$$V_o(t) = V_R(t)\left(1 + \frac{C_i}{C_L}\right) + \frac{1}{(R/\!/R_i)\,C_L}\int_0^t V_R(t)\,dt + V_c(0) \quad (1)$$

where C_i and R_i are the input capacitance and resistance of the oscilloscope and $V_c(0)$ is the initial voltage across the loadcapacitor. Since the oscilloscope digitizes and stores $V_R(t)$ as well as performs the indicated mathematical operations, the result $V_o(t)$ can be conveniently displayed on the screen.

RESULTS

The a-Si:H TFTs measured had an inverse staggered electrode structure with chromium gate, and plasma-enhanced chemical vapor deposited SiN_x and a-Si:H. Phosphorus ion implants were used for the source and drain contacts and Al–Si was used for the source and drain metal. The oscilloscope used for the measurement was a Tektronix 11401 Digitizing oscilloscope. It has an input impedance R_i of $1\,M\Omega$ and input capacitance C_i of 15 pF. It will be discussed below, that the resistor R was chosen so that it is much smaller than R_i and hence R_i was ignored during the calculations. The input capacitance of the scope does not change the circuit response because the first term in eqn (1) is much smaller than the second term. Thus, eqn (1) was simplified by neglecting R_i and C_i. For the TFT inverter, care should be taken in choosing the value of the resistor, R. Firstly, the resistor should not be too small so that it is difficult to accurately measure the voltage drop across it. Secondly, it should not be too large that it alters the charging or discharging resistance, and thus, change the circuit response. A $33\,k\Omega$ resistor and 20 pF capacitor was used for the measurements discussed below.

It is very important to remove any noise in the system or offset in the measurement of $V_R(t)$ because any unwanted d.c. voltage, when integrated, will result in a line of constant slope superimposed on the desired waveform. The voltage $V_R(t)$ was measured over one complete cycle and averaged over 512 measurements by the oscilloscope. Spikes in $V_R(t)$ were observed at instants when the input voltage was switched. $V_R(t)$ was stored in the oscilloscope and then the simplified form of eqn (1) was used to calculate $V_o(t)$, as shown in Fig. 2.

The major unknown in the measurement was to determine the initial condition, $V_c(0)$. It is the ON voltage across the driver TFT and also the voltage to which the load capacitor discharges when the input to the circuit is high. $V_c(0)$ cannot be measured during the dynamic operation of the inverter. However, it can be accurately measured under static conditions using a high quality d.c. electrometer. The static value of $V_c(0)$ can be used in the dynamic measurement provided the charge trapping hysteresis is not significant. In this case, the static characteristics do not differ significantly from the dynamic characteristics. The devices used in the inverter circuit were fabricated at our facility and exhibited excellent characteristics with little charge trapping. $V_c(0)$ was measured using a Keithley 619 Electrometer/Multimeter ($R_i > 10^{14}\,\Omega$). The value of $V_c(0)$, obtained 5 s after the gate input was pulsed, was 5.3 V (the value used in Fig. 2).

CHARGE TRAPPING

The measurement of $V_c(0)$ under static conditions was justified by examining the charge trapping in the TFTs. a-Si:H TFTs have a high density of localized states in the bulk semiconductor and at the semiconductor–insulator interface. Upon the application of a bias, charges are trapped in these states and the current through the device decays with time. Figure 3 shows the decay in the drain–source current upon the application of a gate pulse measured versus time. The initial exponential decay (top curve) is much larger than the subsequent decay (bottom curve). The fast decay can be attributed to states in the bulk a-Si:H while the slow decay is due to the interface states[3]. With the drain and gate bias of 18 V, the current decreases

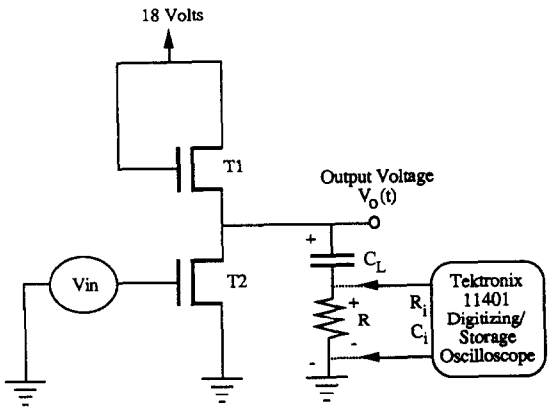

Fig. 1. An a-Si:H TFT enhancement load inverter circuit. $C_L = 20$ pF, $R = 33$ K, $R_i = 1$ MΩ, $C_i = 15$ pF. T1 and T2 have W/L ratios of 95/1 and 38/1, respectively.

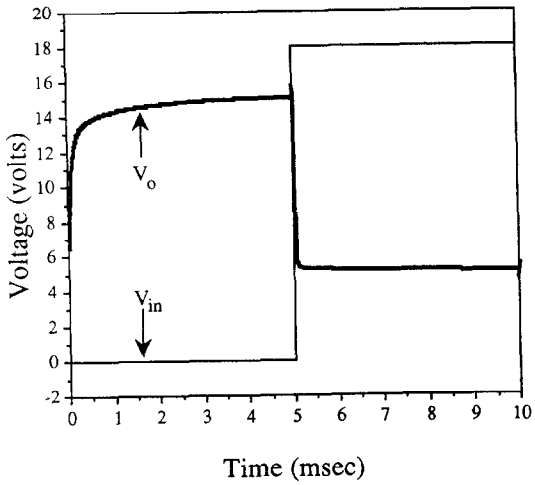

Fig. 2. The input voltage applied to the gate of the driver TFT and the output voltage, $V_o(t)$, of the inverter calculated from the simplified form of eqn (1).

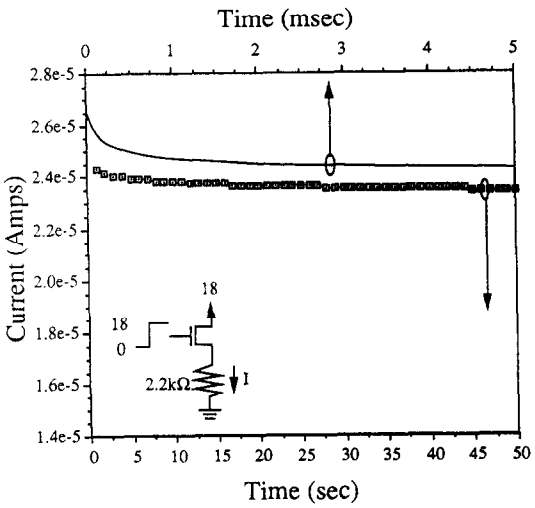

Fig. 3. The current decay in TFT (T2 in Fig. 1) due to charge trapping upon the application of a gate voltage step. The top and bottom waveforms correspond to different time scales. Inset shows the circuit used to measure these waveforms.

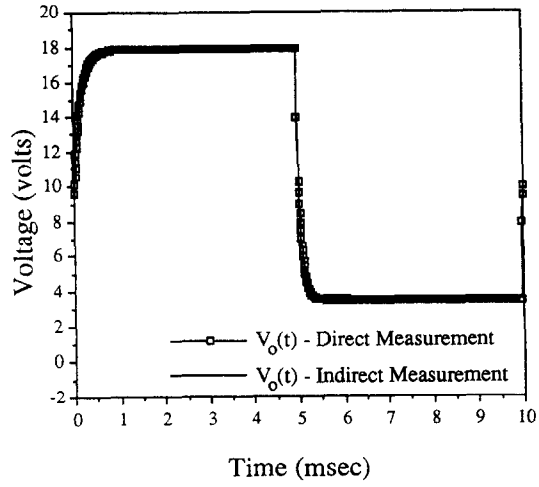

Fig. 4. The excellent agreement of the direct and indirect measurement of the output voltage $V_o(t)$ using a MOSFET inverter circuit.

during the first 5 ms by only 8.6% contributing to a decrease of about 9.6% in 5 s. These values of current decay are much smaller than values reported in literature[3, 4]. The decay in current from 5 ms to 5 s is only different by 1% of the intial current value. This small difference in current in the TFTs does not result in a significant difference in the value of $V_c(0)$ from 5 ms to 5 s. Therefore, the measurement of $V_c(0)$ using the electrometer is justified.

To verify the proposed technique, commercial MOSFETs were placed in a circuit similar to Fig. 1. The output resistance of MOSFETs is small and $V_o(t)$ could be measured directly and compared to the indirect technique. The agreement was found to be excellent as shown in Fig. 4. In addition, a computer simulation of the circuit shown in Fig. 1 using TFT I–V data and experimental results also showed very close agreement.

CONCLUSIONS

An indirect technique was presented to measure the dynamic response of a-Si:H or polysilicon TFT circuits. The indirect technique must be used when the output of the circuit is to be measured in parallel with the output of the TFT where an oscilloscope can not be directly used due to the TFTs high output impedance ($\approx 10^{12}\,\Omega$). We determined that the charge trapping in the TFTs did not affect the measurement technique. The proposed technique was applied to obtain the output waveform of an enhancement-type a-Si:H TFT inverter circuit with a capacitor load, a circuit configuration which will occur in the LC display and circuit technology.

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