PLATOP: A Novel Planarized Trench Isolation and Field Oxide Formation Using Poly-Silicon

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***Abstract*—A novel isolation scheme named planarized trench isolation and field oxide formation using poly-silicon (PLATOP) is described. PLATOP is applicable to high-performance submicron VLSI since it results in encroachment-free shallow trenches, and planarized field oxide. The process offers poly-silicon-filled deep trenches. The process also relies on noncritical lithography and novel etch processes to planarize the deposited poly-silicon from the top of the active areas, and oxidation to consume the poly-silicon in the field regions. Electrical results are presented proving the viability of the isolation scheme.**

I. Introduction

As the semiconductor industry moves into the manufacturable submicron era, the need for a planar submicron isolation process is increased. The process should be applicable to high-density and -performance CMOS/bipolar processes, and should not suffer from the conventional limitations of LOCOS-based isolation. In addition, deep trench isolation is finding abundant use in semiconductor processes to increase packing density and latch-up immunity. Many processes have been reported in literature in the past years [1]–[3]. The reported processes to date have the following difficulties and limitations: a) lateral encroachment due to the formation of birds beak (nonlithography limited); b) increased difficulty to form thick oxides (>1 μm); c) increased difficulty to combine deep trench and field isolation; and d) use of techniques such as CMP or resist planarization which are more susceptible to area and loading effects.

The purpose of this work is to develop a fully walled, planar isolation scheme which is compatible with deep trench isolation [4]. The process allows for thick field oxides, results in a planar surface, and results in walled junctions. Test structures were fabricated to measure the junction leakage currents and breakdown voltages to establish the feasibility of the process.

II. Process Flow

Isolation test structures were fabricated on p ⟨100⟩ substrates with 12–15 Ω-cm resistivity. After the formation of antimony doped n^+ buried layers, a 2.2 μm, 1 Ω-cm epitaxial layer was grown on the wafers. n^+ sinker regions were then formed by phosphorus ion implantation. Using a photoresist mask, 1.4 μm of silicon was etched to form the shallow isolation trenches. A sacrificial 2.0 μm plasma-enhanced TEOS-based oxide (PETEOS) was deposited and etched to define the location of the deep trenches as shown in Fig. 1(a). The deep trenches were then etched in an AMAT5000 etcher using the PETEOS as the hardmask. The PETEOS hardmask was stripped using a wet-etch and a thin 600 Å sacrificial oxide was grown at 1050°C to remove any defects from the RIE etching. The thin oxide was stripped off and a 1100 Å oxide was regrown to passivate the trench sidewall. A 1300 Å Si_3N_4 and 0.5 μm thick poly-silicon layer was then deposited. The poly-silicon layer also filled the 1.2 μm wide and 20 μm deep trenches as shown in Fig. 1(b).

Next, a 2.0 μm LTO layer was deposited over the wafer and etched back to leave spacers on the side of the poly-silicon. Subsequently, a photoresist mask was aligned so that the edges of the resist were situated within the spacers as shown in Fig. 1(c). The width of the spacer is much larger than the alignment tolerance. A 60 W, 450 mTorr, SF_6 plasma was used to etch the polysilicon isotropically from the top of the active areas using the photoresist and the oxide spacers as the mask. The etch rate selectivity of (oxide, resist, nitride): poly-silicon <1:10. The poly-silicon was etched long enough so that the poly-surface was left planar as shown in Fig. 1(d). Photoresist and oxide spacer were stripped and the poly-silicon was oxidized at 1050°C in wet ambient for 3.5 h resulting in a planar oxide as shown in Fig. 1(e). Boron was implanted through the nitride and oxide and a thermal cycle was used to form p^+/n diodes in the active device regions. Dry etch of the nitride/oxide was performed and metallization was done to make contacts to the devices as shown in Fig. 1(f).

III. Results and Discussion

Fig. 2 shows the final SEM cross section of a typical device showing 20 μm deep poly-filled trenches lined with oxide and nitride. For the purpose of this experiment, the poly was not completely consumed. Fig. 3 shows the p^+/n diode forward current and ideality factor of 1.02 indicating excellent material quality. Fig. 3 also shows the leakage current through the p^+/n diode formed in the active area with a breakdown voltage of 35 V. Also shown is the isolation breakdown (n^+ to n^+) through the deep trench showing low leakage and breakdown voltage of 52 V. The high breakdown and low leakage characteristics indicate excellent material quality close to the shallow and deep trench areas proving that there are no defects generated from the poly-silicon oxidation.

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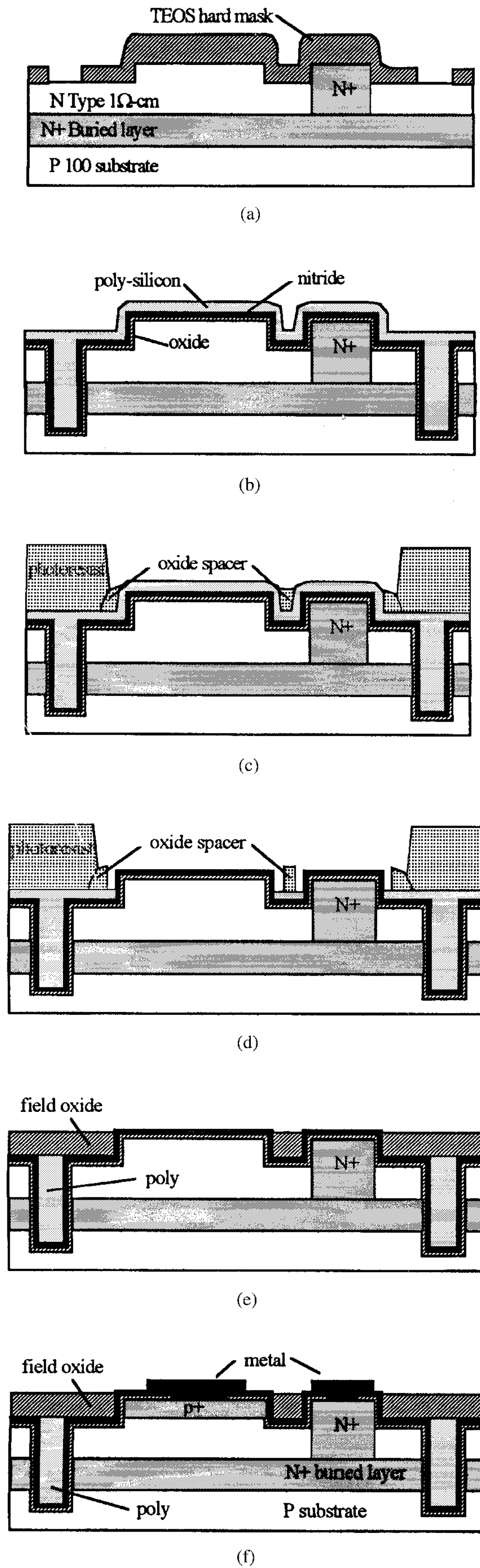

Fig. 1. Process flow cross sections of the isolation test devices.

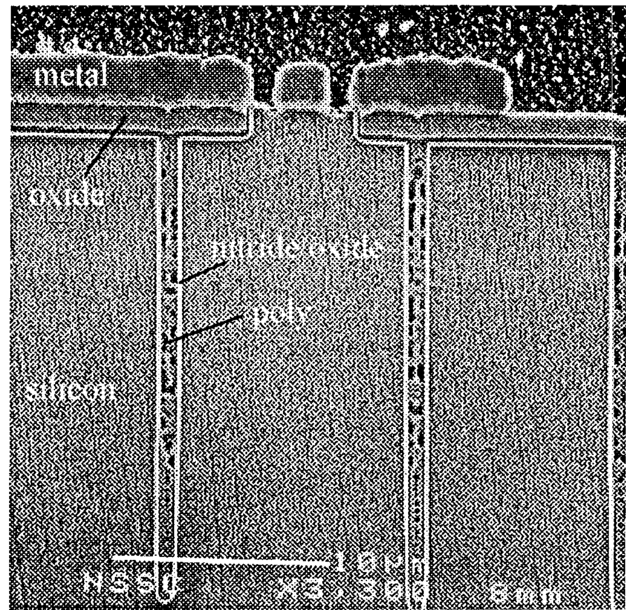

Fig. 2. SEM cross section of the deep trench isolated test structure.

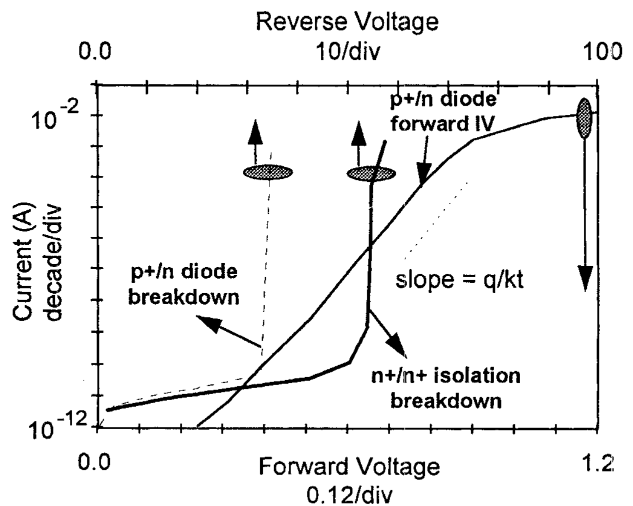

Fig. 3. Plot showing the p^+/n diode current, ideality factor, breakdown voltage and n^+n^+ isolation breakdown voltage.

IV. Conclusions

A novel isolation scheme named PLATOP is described. The process relies on noncritical lithography, novel etch process, and oxidation to form planar and encroachment free field oxide and device regions. Electrical results show excellent breakdown characteristics proving the viability of the isolation process. Future work is underway to characterize the process and structures in more detail.

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