Characterization and modeling of sidewall defects in selective epitaxial growth of silicon

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The sidewall defects in selective epitaxial growth (SEG) of silicon were characterized and the nature of these defects was investigated. Electrical characterization of the sidewall defects was performed using diodes fabricated in structures using the SEG of silicon and chemical-mechanical polishing. Diodes were fabricated with various perimeter to area ratios to extract the bulk and sidewall saturation current densities and ideality factors in as-grown SEG diodes and reoxidized sidewall SEG diodes. Transmission electron microscopy was used to show that nitrogen annealing of the sample with the sidewall oxide removed exhibited a dramatic decrease in the sidewall defects as compared to the sample with the sidewall oxide present during the anneal. The generation of the defects was attributed to stress due to the mismatch in thermal expansion coefficients of oxide and silicon and a model describing the generation of these defects was formulated and described.

I. INTRODUCTION

Selective epitaxial growth (SEG), epitaxial lateral overgrowth (ELO), and confined lateral selective epitaxial growth (CLSEG) of silicon have been identified as key technologies for the next generation of very large scale integrated/ultralarge scale integrated circuits (VLSI/ULSI) which will use novel three-dimensional (3D) bipolar, metal–oxide–semiconductor, bicomplementary metal–oxide–semiconductor, and silicon-on-insulator (MOS, BiCMOS, and SOI, respectively) devices.[1–5] The bulk SEG silicon is of excellent quality but the material close to the sidewall insulator can have a high defect density. The presence of defects along the sidewall has been reported earlier.[6–8] The presence of the sidewall defect is considered to be the most important problem hindering the widespread use of SEG in semiconductor processing because junctions and depletion regions intersecting these sidewall defects will result in undesirable recombination–generation (R–G) currents. Hence, it is extremely important that the nature of these defects be investigated and understood.

The nature of the SEG sidewall defects was investigated using a particular structure, namely, a submicron width trench isolation technique that has been reported earlier by many researchers. Kurten *et al.* have presented this isolation technique for MOS and bipolar applications.[9–13] The process sequence for the SEG isolation is much simpler than the process for local oxidation of silicon (LOCOS) isolation and eliminates the lateral encroachment due to the bird's beak effect. An improvement of the SEG isolation structure used to investigate the sidewall defects in this article is that it results in a planar surface by using chemical-mechanical polishing (CMP). The planarity of the top surface is a property that is highly desirable with the increasing use of multilevel metal schemes.

It is the purpose of this article to characterize and model the sidewall defects in the selective epitaxial growth of silicon. The defects were electrically characterized by fabricating diodes in a submicron width trench isolated structure using SEG and chemical-mechanical polishing with junctions intersecting the sidewall interface of interest. Bulk and perimeter ideality factors and saturation current densities were extracted to characterize the bulk and sidewall SEG material. Transmission electron microscopy and various anneal experiments were used to study the nature and origin of the defects. Based on the results of the experiments, a one-dimensional model describing the generation of these defects due to thermal stress was formulated and described.

II. DEVICE STRUCTURES

Four different structures were used to study the sidewall defects in SEG. The fabrication process for these structures is described below.

A. Process A—as grown

The cross sections of the process sequence are shown in Fig. 1. The fabrication process started with *n*-type 1–5 Ω cm, {100} silicon wafers. The device structures were oriented along the ⟨100⟩ direction on the {100} plane to reduce defects and enhance the material quality. The process began by growing a 0.38 μm layer of field oxide on the silicon. Photoresist mask was then used to form a trench by anisotropically etching through 0.38 μm of oxide and 2.5 μm of silicon in Freon 115 plasma. A wet oxidation that was performed at 1000 °C resulting in a 0.27 μm layer of oxide on the sidewall and bottom of the trench. Next, a maskless anisotropic reactive ion etch (RIE) was used again to etch the oxide from the silicon substrate and open the seed hole for SEG/ELO. The wafers were annealed at 1000 °C for 10 min in dry N_2 to remove the RIE damage. A thorough wafer clean

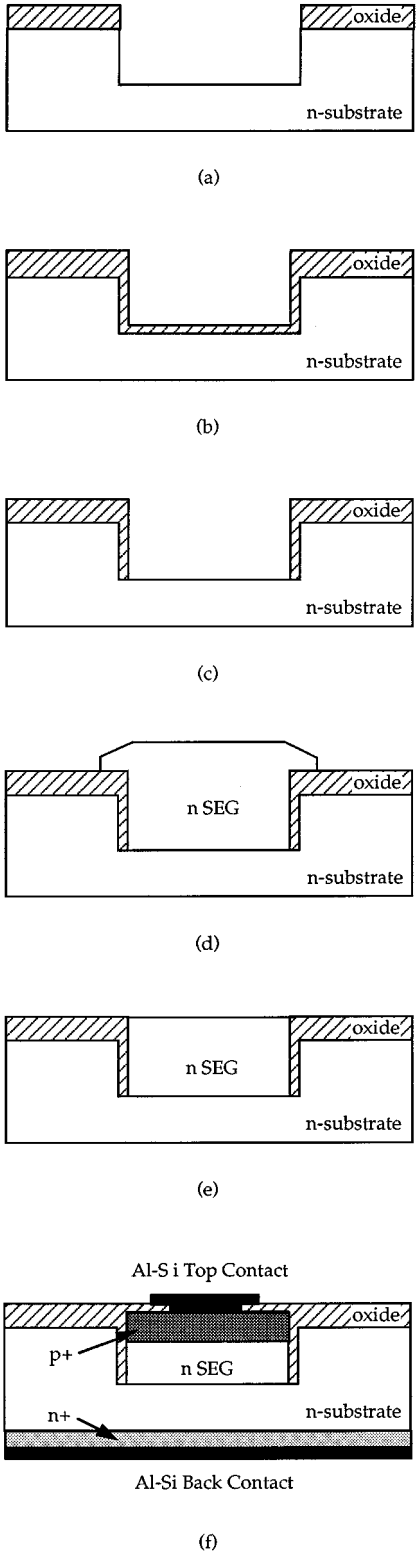

FIG. 1. Process flow for the fabrication of the diode to study the SEG sidewall defects.

and buffered hydrofluoric acid (BHF) dip was performed prior to SEG/ELO of silicon. Next, SEG/ELO of silicon was performed in a standard reduced-pressure pancake-type rf-heated epitaxial reactor. A 5 min hydrogen bake and 30 s HCl etch, both at 970 °C, were used prior to growth. SEG/ELO was then grown from the silicon seed holes at 970 °C and 40 Torr at a growth rate of ≈0.12 μm/min to result in 4.0 μm of growth. The growth did result in silicon material over the field oxide and hence a planarization step was needed. The wafer was chemical-mechanically polished down to the surface using the field oxide as an etch stop. The active device region isolated by the substrate by a submicron width insulator is now ready for MOS or BJT fabrication. The SEG/oxide sidewall was characterized by p^+/n diodes fabricated in the active device regions. After the CMP, boron was implanted in the devices for diode formation at an energy of 25 keV and a dose of 3×10^{13} cm^{-2}. The back of the wafer was implanted with arsenic at an energy of 35 keV and a dose of 3×10^{15} cm^{-2}. The implants were driven in by growing a wet oxide for 14 min at 1000 °C. Contacts were opened and approximately 0.25 μm of Al–1% silicon alloy was sputtered deposited and defined using liftoff. The wafers were finally annealed at 415 °C in dry N_2 for 20 min.

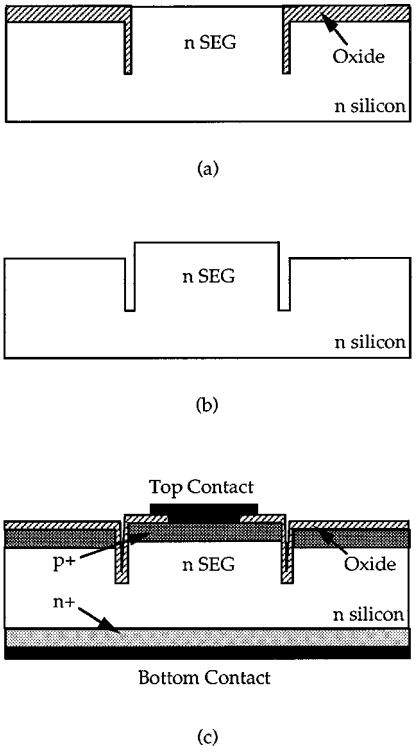

FIG. 2. Process flow for the reoxidized diode.

B. Process B—reoxidized

To examine the effect of reoxidation, the following experiment was performed. After chemical-mechanical polishing the SEG/ELO, the wafers were placed in HF to completely remove the sidewall oxide as shown in Fig. 2. The wafers were then reoxidized at 1100 °C for 40 min in dry O_2 to result in about 0.11 μm of oxide. The wafers were placed in BHF for 45 s to reduce the top oxide thickness. The top diode and back contact was then formed on the wafer exactly the same as the as-grown process A.

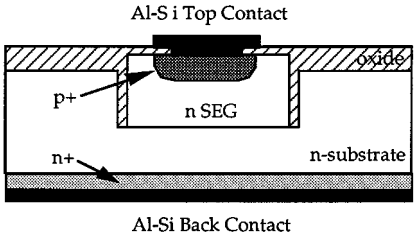

FIG. 3. Cross section of the control diode in SEG with base junction 6 μm away from the sidewall oxide.

C. Process C—LOCOS

Conventional LOCOS isolated diodes with junctions intersecting the LOCOS sidewall were fabricated and used as control devices. The implants and activation cycles used were identical to the other two processes.

In addition to the above three structures, SEG control diodes were fabricated in the SEG material using a mask with junctions 6 μm away from the sidewall oxide, once the SEG/ELO was chemically mechanically polished. This sample would indicate the quality of the bulk SEG material. The cross section of this diode is shown in Fig. 3.

III. ELECTRICAL CHARACTERIZATION

Figure 4 shows the $I-V$ characteristics of the SEG control diode where the junction was 6 μm away from the sidewall oxide. This result indicates that the bulk SEG material quality is excellent and that there are no defects 6 μm away from the sidewall oxide as shown by the excellent ideality factor of approximately 1.0. The forward bias $I-V$ curves of as-grown and reoxidized diodes are shown in Fig. 5. The ideality factor of sample C is about 1.78, indicating high recombination in the space charge region (SCR). These diodes had the junctions intersecting the sidewall, and hence it can be inferred that the sidewall defects are the main cause of the poor ideality factor. Also shown in Fig. 5 is the $I-V$ curve for the reoxidized sample. The reoxidation step has removed some of the defects and the ideality factor has decreased to about 1.4 at 0.5 V.

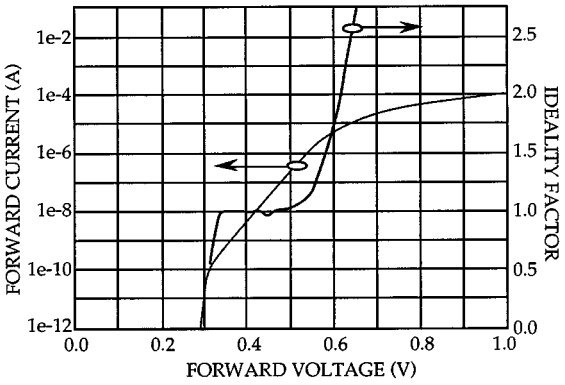

FIG. 4. Forward $I-V$ characteristics and ideality factor of control SEG diode with junctions 6 μm away from the sidewall oxide, $\eta \approx 1.00$.

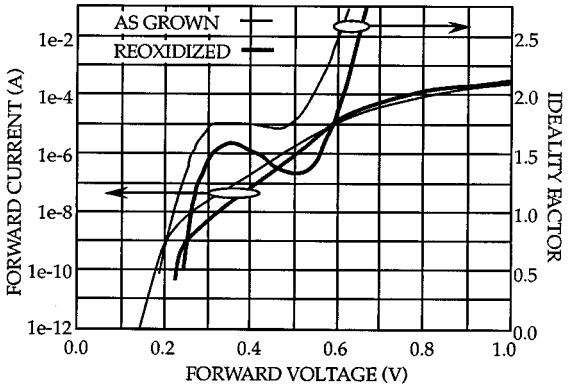

FIG. 5. Forward $I-V$ characteristics and ideality factor of the as-grown and reoxidized processes.

A. Characterization technique

The current through a diode in the forward bias region is the sum of a diffusion component and a recombination current. The recombination current is characterized by the ideality factor η, theoretically equal to 2. The recombination current is dominant at low forward biased applied voltages while the diffusion current dominates at higher voltages. The diffusion and recombination current can be lumped together, and the perimeter current component can be included to obtain the total diode current as shown in Eq. (1):

$$I = AJ_{b0}\left[\exp\left(\frac{qV}{\eta_b kT}\right)-1\right]+PJ_{p0}\left[\exp\left(\frac{qV}{\eta_p kT}\right)-1\right]. \quad (1)$$

In Eq. (1), A is the diode area, J_{b0} is the bulk saturation current density (in A/cm^2), η_b is the bulk ideality factor, P is the perimeter of the diode, J_{p0} is the perimeter saturation current density (in A/cm), η_p is the perimeter ideality factor, and V is the applied voltage. Dividing the resultant equation by the area results in the following Eq. (2):

$$J = J_{b0}\left[\exp\left(\frac{qV}{\eta_b kT}\right)-1\right]+\frac{P}{A}J_{p0}\left[\exp\left(\frac{qV}{\eta_p kT}\right)-1\right]. \quad (2)$$

Thus, for a given voltage, if the measured current density is plotted as function of the perimeter to area ratio, a straight line should be obtained with the slope given by the perimeter current component and the x intercept given by the bulk current component. If the measurement is performed at two different voltages between which the ideality factor is assumed to be constant, then two values of slopes can be obtained as shown in the following two equations:

$$\text{slope } 1 = J_{p0}\left[\exp\left(\frac{qV_1}{\eta_p kT}\right)-1\right], \quad (3)$$

$$\text{slope } 2 = J_{p0}\left[\exp\left(\frac{qV_2}{\eta_p kT}\right)-1\right]. \quad (4)$$

The last two equations can be solved simultaneously to obtain the values of J_{p0} and η_p. This technique has been applied on GaAs diodes and solar cells to study the effect of perimeter recombination.[14] The bulk current components can be obtained by dividing Eq. (1) by the perimeter to obtain Eq. (5):

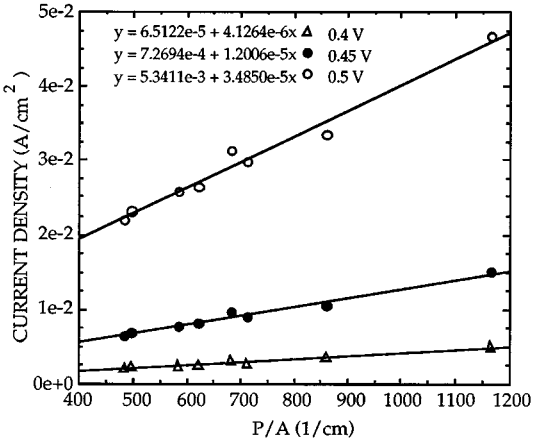

FIG. 6. A representative J vs P/A plot for as-grown diode.

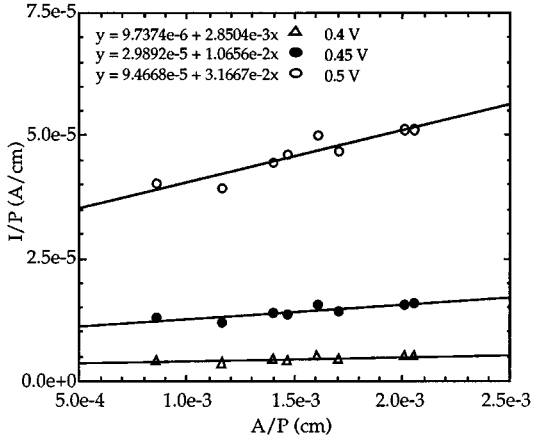

FIG. 7. A representative I/P vs A/P plot for as-grown diode.

$$\frac{I}{P}=\frac{A}{P}J_{b0}\left[\exp\left(\frac{qV}{\eta_b kT}\right)-1\right]+J_{p0}\left[\exp\left(\frac{qV}{\eta_p kT}\right)-1\right]. \quad (5)$$

Thus bulk current components can be obtained from the slope of the least-squares fit of an I/P vs A/P plot. Taking the data at two different voltages allows for the extraction of J_{b0} and η_b, which characterize the bulk current component.

B. Sidewall characterization

The sidewall of the diodes was characterized by the method described above. The current through each of the diodes was measured at three different voltages where the ideality factor was constant. The measured current was divided by the area and the current density obtained was plotted versus the perimeter to area ratio. The least squares fit of the data was used to obtain the slope. Two different values of slopes were used to solve for the sidewall parameters, η_p, and J_{p0}. Figure 6 shows a representative P/A plot for the as-grown diodes. 20 dies containing diodes of the various areas were tested. Sidewall parameters were extracted for each die and the values were averaged to obtain one value each for parameters, η_p and J_{p0}. In exactly the same manner, sidewall parameters were also obtained for the reoxidized diodes and the LOCOS diodes. The results are listed in Table I.

C. Bulk characterization

To obtain the bulk parameters, η_b and J_{b0}, and for the diodes, I/P was plotted as a function of A/P. Again, the slopes at two different voltages were used to extract the bulk parameters. The bulk parameters will include the contribution from the defects as long as the defects are not at the sidewall interface. The results of process B (the SEG control diode) indicated that the majority of the defects were somewhere within 6 μm of the sidewall interface. This means that any defects originating from the sidewall and within 6 μm away will increase the ideality factor even though the central SEG material is defect free. Thus the bulk ideality factor η_b and saturation current density J_{b0} are not representative of the entire SEG bulk region. A representative I/P vs A/P plots for the as-grown diode is shown in Fig. 7. The results are listed in Table I.

TABLE I. Summary of electrical results for the sidewall defect study.

Device	η at 0.45	η_p	J_{p0} (A/cm)	η_b	J_{b0} (A/cm^2)	J_{rev} (A/cm^2) at -3.0 V
LOCOS diodes	1.02	1.00	4.35×10^{-14}	1.05	4.04×10^{-11}	2.03×10^{-7}
As-grown diodes	1.78	1.83	1.00×10^{-9}	1.40	1.28×10^{-8}	4.20×10^{-3}
Reoxidized diodes	1.40	1.37	2.24×10^{-11}	1.38	5.57×10^{-9}	6.00×10^{-3}

D. Reverse leakage measurement

The reverse leakage current of the diodes were also measured in order to further characterize the devices. The measurement was performed at -3 V using a Hewlett–Packard picoampmeter. Figure 8 shows the histograms of the leakage currents.

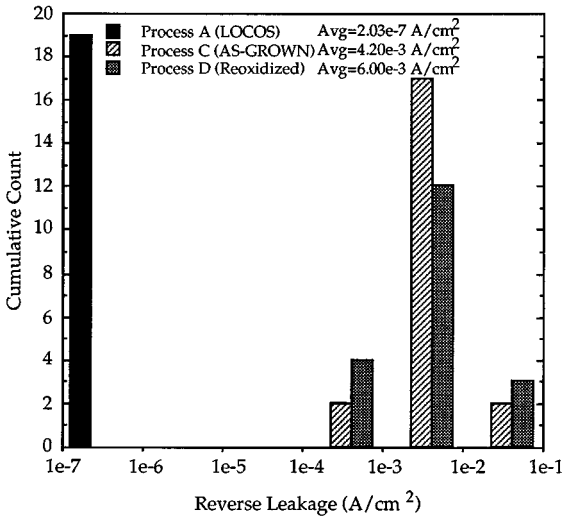

FIG. 8. Histograms of the leakage currents.

TABLE II. Surface recombination velocities and lifetimes.

Device	S_0 (cm/s)	τ_0 (μs)
LOCOS diode	6.06	178
As-grown diode	1.39×10^5	0.56
Reoxidized diode	3.12×10^3	1.29

E. Discussion of results

In the above sections the characterization results of the different diode structures were presented. The LOCOS diode shows excellent ideality factors showing minimum recombination in the SCR region. The LOCOS process shows the minimum ideality factors, saturation current densities, and reverse leakage, as expected. The five orders of magnitude increase in the perimeter saturation current density and three orders magnitude increase in the bulk saturation current density in the as-grown diode, respectively, indicate the presence of many defects within 6 μm of the sidewall. The reoxidation procedure decreased the ideality factors and saturation current densities. As indicated by the results, the defects have been reduced but not eliminated by the reoxidation procedure. The perimeter defects were decreased more than the bulk defects. This could have been due to two reasons. Firstly, a longer oxidation time might be required to further reduce the bulk defects and the oxidation time used simply might not have been long enough. Secondly, it is possible that the reoxidation of the narrow groove might have induced dislocations in the bulk in spite of reducing the already existing defects after the SEG growth. The perimeter defects were reduced simply because the reoxidation produced a new interface with the SEG, hence, healing any interface damage and filling up the dangling bonds and reducing the interface state density. The reverse leakage current of the SEG isolation devices were four orders of magnitude larger than the LOCOS device. The application of -3 V was appropriate because the depletion width was within the SEG and did not extend in the substrate as confirmed by PISCES-2B device simulations. The nature and type of these defects are discussed in the next section with the aid of transmission electron microscopy.

The values of J_{p0} and J_{b0} from Table I can be used in Eqs. (9) and (10) to calculate values of the W/τ_0 and S_0L_p. τ_0 is the lifetimes in the bulk and S_0 is the surface recombination velocity. Using an approximate value of W and L_p as 448 Å obtained from the PISCES-2B simulator, S_0 and τ_0 can be calculated. The values are listed in Table II. As expected, the value of S_0 is the lowest for process A and the highest for process C. Reoxidation decreases the value of S_0 by two orders of magnitude. The increase in τ_0 after reoxidation is not as pronounced as the decrease in S_0.

IV. MATERIAL CHARACTERIZATION

In this section, transmission electron microscopy (TEM) was used to observe and characterize the defects in the SEG. Figure 9 shows a TEM micrograph taken from a sample from an as-grown diode. Defects were mostly generated within 1 μm from Si/SiO_2 interface, while a defect-free region was found away from the sidewall. This fact was already predicted by the near perfect ideality factors of the control SEG diodes. Dislocations observed farther away from the sidewall were believed to have been driven a certain distance from the sidewall by stresses. By comparing images that show that all of the dislocations in process C sample are simultaneously out of contrast under 400 and 3-11 reflections, it was concluded that these dislocations were the same perfect type and with Burgers vector in [110] direction, which makes an angle of 45° with respect to the sidewall.

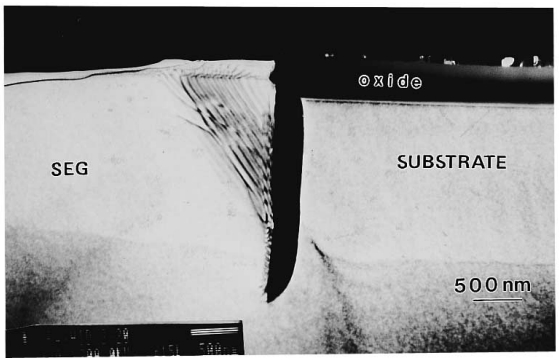

FIG. 9. TEM micrograph of as-grown diode showing the defects.

Figure 10 is a TEM micrograph taken from a sample of the reoxidized diode. The oxide shown did not fill up the cavity region. This is due to the fact that a BHF etch was performed to reduce the top oxide thickness. It is to be noted that an obvious reduction of defects was observed in this sample. The scattered dislocations, the only defects observed in this sample, were formerly bounded at one end to the sidewall interface, and propagated from the interface into both the epilayer and the substrate. This is distinct from the observation of the as-grown diode, in that the dislocations were only formed in the epilayer. The dislocation images nearly vanished under the same reflections as those for as-grown diode process A, and the identified the Burgers vector to be of the type [110]. Although the high temperature treatment may anneal out defects produced from SEG growth, the stresses induced by the oxidation of the narrow groove may introduce new defects into the SEG layer. This was probably

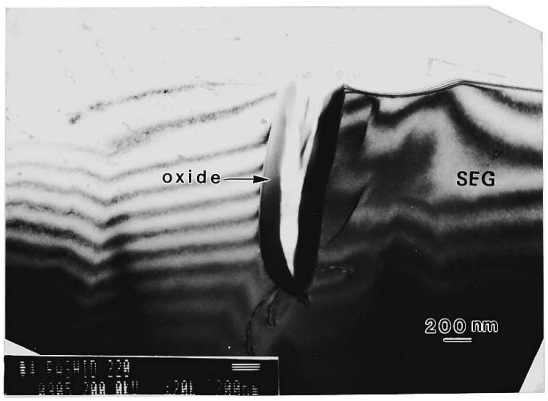

FIG. 10. TEM micrograph of the reoxidized diode showing the dramatic reduction of defects in the SEG.

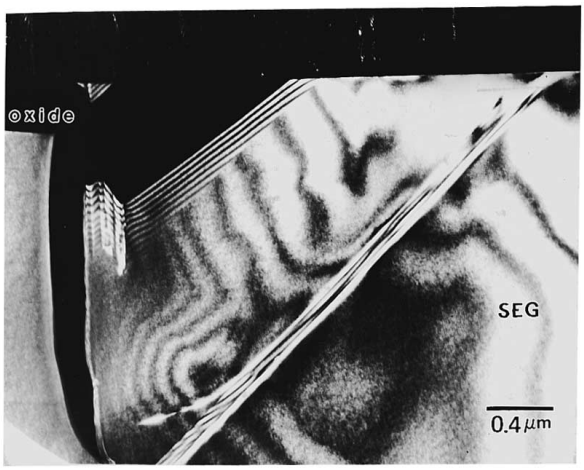

FIG. 11. Dark field TEM micrograph taken from process 1.

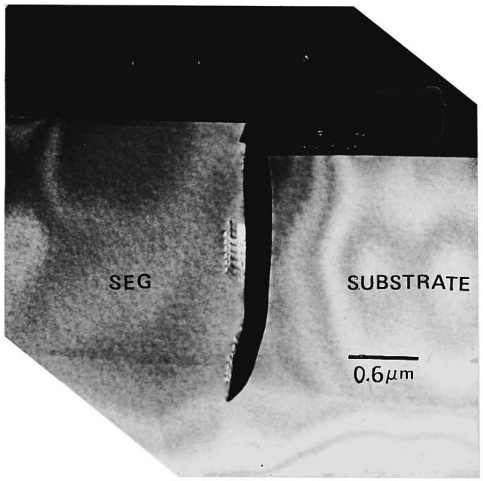

FIG. 12. Dark field TEM micrograph taken from process 2.

the cause of the dislocations seen in the sample from the reoxidized diodes, originating from the bottom of the narrow groove.

Two more experiments were done to investigate the sidewall defects. In the first experiment (named process 1), samples were taken after the chemical-mechanical polishing and were subjected to annealing in N_2 ambient at 1100 °C for 40 min, which is the same time and temperature as the reoxidation step in the reoxidized diode described above. In the second experiment (named process 2), samples were taken after the chemical-mechanical polishing and the oxide was completely removed by wet HF etching. Then an anneal in N_2 ambient at 1100 °C for 40 min was performed with the oxide absent. For TEM observation, low-pressure chemical vapor deposition (LPCVD) polysilicon at 600 °C was used to fill up the cavity region solely to protect the sidewall region during ion milling. The structure of process 1 was examined and is shown in Fig. 11. The stacking faults are still the major defects in the SEG. One of them originated from the SEG sidewall interface and propagated at about 45° through the epilayer, ending at the SEG surface. The other defects appeared similar to those in the as-grown diode, including dislocations and stacking faults. By comparing the samples of as-grown diode and process 1, it may be seen that the defect densities were only slightly reduced by nitrogen annealing. For process 2, it was evident that most of the defects were eliminated, as shown in Fig. 12. The defects observed in sample 2 were mostly dislocations, and these dislocations formed an array near the sidewall interface.

Samples from processes 1 and 2 were annealed at the same condition except that sample 1 was annealed with the existence of the sidewall oxide, but sample 2 was annealed without the presence of the oxide. High temperature annealing of the SEG material may be able to remove defects caused by growth mistakes and thermal expansion (resulting from SEG growth); however, new thermal stresses will be generated in the sidewall region during the cool-down period. The new stresses will generate new defects, and these defects should have about the same nature as those for the as-grown process without annealing, which is the case. For process 2, high temperature annealing would remove any defects in the SEG. During the cool-down period of the anneal, however, thermal stress due to the mismatch in coefficient of expansion will not be generated because of the absence of the oxide. Further longer annealing may possibly cleanse the residual dislocations in process 2. This experiment gives evidence to understand defect formation near the sidewall interface, and a way to minimize defect densities.

V. MODELING OF THE SIDEWALL DEFECTS

A. SEG/ELO sidewall defects

Various authors have discussed the possible causes for the SEG sidewall defects.[1–9] It is postulated that the main cause of the SEG/ELO sidewall defects is thermal stress after the SEG growth during the cool-down period.[2] This postulate is also confirmed by our experiments for the first time. The oxide/silicon interface is a location of high internal strain. As a strain relief mechanism, stacking faults are generated in the silicon material. The strain could be introduced as a result of the difference in thermal coefficient of expansion between the silicon overgrowth and the oxide. At high temperatures, the silicon yield strength is lowered and the thermal stress could exceed the material yield strength. If this situation occurs, the internal stress will be relieved by plastic deformation of silicon.[15–18] The thermal stress could also be reduced if the thermal coefficient of expansion of the insulator next to the overgrowth is matched to that of silicon.

B. Yield strength of silicon

The mechanical properties of silicon, just like most other materials, is described by a stress versus strain curve.[15] The sample obeys Hook's law until the stress reaches the upper yield strength (σ_{uy}). Above this value, silicon starts to plastically deform. Dislocations and stacking faults will be induced and the sample will not return to its original shape after the removal of the forces. Further increase in strain reduces the stress rapidly to a level designated as the lower yield strength (σ_{ly}) followed by a slow increase in the stress with increasing strain. The temperature dependence of the

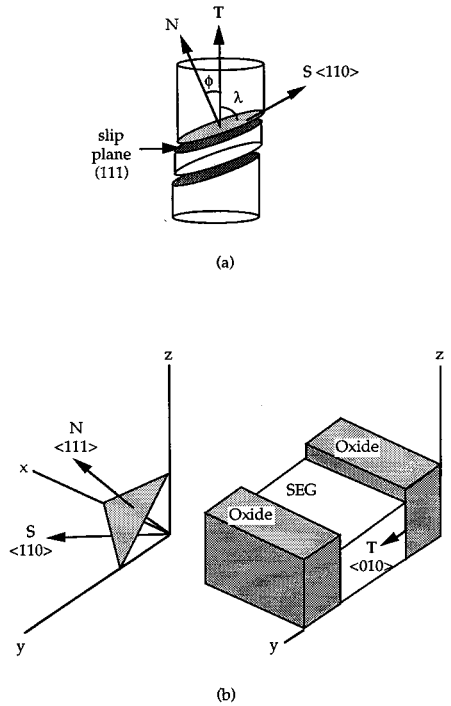

FIG. 13. (a) Illustration of Schmid's law. *N* is the slip plane normal, *T* is the axis of tension or compression, and *S* is the slip plane direction (Ref. 15). (b) The SEG/insulator sidewall and the pertinent vectors for the calculation of the shear stress.

upper yield strength value is of most interest in the present work and it is given by the following equation:

$$\sigma_{\mathrm{uy}} = 1.4\times 10^{-5}\epsilon^{1/2.1}\exp\left(\frac{2.3}{2.1kT}\right). \tag{6}$$

In the above equation, ϵ is the strain rate with units of percent change in specimen length per second ($\Delta L/L$ s). In silicon, dislocation and plastic deformation occurs when the shear stress acting in that slip plane exceeds the above mentioned upper yield strength, σ_{uy}. In silicon, the slip planes are the (111) family of planes and the favorable direction of slip propagation is in the [110] direction.The relationship between the applied stress and the shear stress τ acting along the slip plane is given by Schmid's law [Eq. (7)] and shown in Fig. 13:[15]

$$\tau = \sigma \cos\phi \cos\lambda. \tag{7}$$

Here ϕ is the angle between the normal to the slip direction and the axis of tension and λ is the angle between the slip direction and the axis of tension. The equation above was used for translating the applied stress to the shear stress before it can be compared to the shear thermal stress.

C. Thermal stress

The stress in a film is the sum of the thermal stress σ_t, the intrinsic stress σ_i, and external stress σ_{ex}. For the SEG silicon, the intrinsic stress is assumed to be negligible since single crystal silicon is being grown as a continuation of the substrate.The external mechanical forces imposed on the

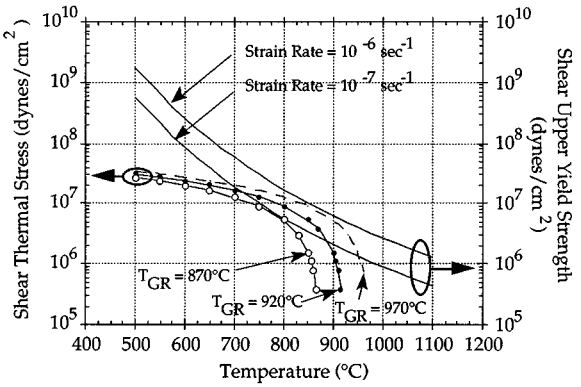

FIG. 14. Shear thermal stress and shear upper yield strength as a function of temperature to predict the defect-free operating range.

SEG during growth are also assumed to be zero. Under these assumptions, the total stress is only the thermal stress, given by the following equation:

$$\sigma_t = \frac{E_f}{1-\nu}\int_T^{T_{\mathrm{GR}}}[\alpha_{\mathrm{Si}}(t)-\alpha_{\mathrm{ox}}(t)]dt, \tag{8}$$

where E_f is the silicon Young's modulus, ν is the Poisson's ratio, α_{Si} and α_{ox} are the coefficient of thermal expansion of silicon and oxide, T_{GR} is the temperature of film deposition, and T is the temperature at which the stress is desired. An experimentally determined expression for the coefficient of expansion for silicon in the temperature range of 0 to 1200 °C is given by Eq. (9):[19]

$$\sigma_{\mathrm{Si}}(t) = (3.725\{1-\exp[-5.88\times 10^{-3}(t+149)]\}+5.548 \times 10^{-4}(t+273))\times 10^{-6}\ (^{\circ}\mathrm{C}^{-1}). \tag{9}$$

The coefficient of expansion of oxide does not change much with temperature and a value of 0.6×10^{-6} °C^{-1} was used to simplify the calculations. Equation (8) can be used to calculate the thermal stress in the silicon as the temperature is decreased from T_{GR}, the growth temperature, to any temperature T. At T_{GR}, the thermal stress would be zero and it will increase as the temperature is decreased. The value of the shear thermal stress at any temperature should be less than the value of the shear yield strength of silicon in order to avoid plastic deformation and defect formation.

D. Model predictions

Figure 14 shows the shear thermal stress calculated using Eqs. (8) and (9) for growth temperatures, T_{GR} of 970, 920, and 870 °C. The thermal stress is zero at the growth temperatures and increases with decreasing temperature. Also plotted is the shear yield strength using Eqs. (6) and (7) with a strain rate of 10^{-6} and 10^{-7} s^{-1}. The figure provides a basic understanding of the defect generation due to thermal stresses alone. It will be desired to keep the entire shear thermal stress curve under the shear yield strength curve in order to prevent plastic deformation. With decreasing growth temperatures, the shear thermal stress curves are shifted to the

left as expected. A low enough growth temperature reduces the thermal stress to values below the yield strength for all values of temperature.

The model describes and predicts the defect generation and presents a way to possibly eliminate defect formation. The results of the model are as expected, i.e., a reduced growth temperature could inhibit the defect generation. It is difficult to predict the exact operating temperatures of no defect generation because of the uncertainty in the strain rate in the SEG/oxide system and the three-dimensional effects in the geometry that would enhance the stresses around corners and edges. The polysilicon nuclei encapsulation during the SEG growth will also decrease the yield strength of the silicon close to the sidewall. The model does describe the trend that has already been observed in experiments.

A very interesting conclusion drawn from the model is that if the strain rate is increased during the cool-down period, then the shear upper yield strength would also increase. An increase in the strain rate during the cool-down period implies an increase in cooling rate. Thus if the wafers were cooled at a very fast rate only in the regime where the shear thermal stress is higher than the shear upper yield strength in Fig. 14, then the yield strength would increase and plastic deformation might not take place. Thus, the SEG would have internal strain but it would not be relieved, which means no plastic deformation or defect generation.

VI. CONCLUSIONS

This article presented an extensive characterization of the defects in SEG at the sidewall oxide interface. The study increased the understanding of the nature of these sidewall defects. The defects were found to be stacking faults originating from the sidewall and extending into the bulk, 1 μm away from the sidewall. The defects were caused mainly due to the difference in thermal expansion of the oxide and SEG and were most probably generated during the cool-down period of the SEG cycle. Reoxidation of the sidewall dramatically decreased the sidewall defects. If the sidewall oxide was removed and an anneal was performed in inert nitrogen, the defects were removed, whereas if the sidewall oxide was not etched off and a nitrogen anneal was performed, the defects were not reduced. The stress induced in the SEG during the cool-down period was more than the elastic yield strength of the material. The stress was then relieved in the form of stacking faults and dislocations.

A one-dimensional model predicting the defect generation based on the shear upper yield strength of silicon and the shear thermal stress due to mismatch in expansion coefficients was formulated and described. The model predicted that lower growth temperatures will reduce the possibility of inducing defects because of reduced thermal stress at the SEG/oxide sidewall interface. It is difficult to predict the exact operating range for defect suppression based on this model because of the uncertainty in strain rate during the cool-down period after SEG, high stress induced due to three-dimensional effects, oxide degradation, and polysilicon encapsulation during growth. The model provides for a basic understanding of defect generation and shows the correct trends. A way to suppress defects is postulated by increasing the cooling rate in the regime where the thermal stress is higher than the yield strength of silicon. Another interesting possibility could be the use of nitrided oxides as the sidewall insulator. Since the thermal coefficient of expansion are of the following order, $SiO_2 < Si < Si_3N_4$, nitridation of oxides might increase its thermal coefficient of expansion and make it closer to that of silicon. Thus the thermal stress at the interface would be reduced.

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