# A Simple Process to Produce a High Quality Silicon Surface Prior to Selective Epitaxial Growth

R. Bashir, *Member, IEEE,* W. McKeown, and A. E. Kabir

***Abstract*—A simple and low-cost process was devised to eliminate etch damage resulting from oxide etching on the seed-hole surface prior to selective epitaxial growth (SEG) of silicon. The process consists of a low power $C_2F_6$ RIE step which was performed right after the oxide etch step in the same etch reactor. The use of this step excluded the need of a conventional sacrificial oxide to remove damaged silicon regions and residual polymers. The $N/P$ diodes resulting from $N$-type SEG grown on $P$-type substrate were used to evaluate the quality of the silicon surface prior to SEG.**

## I. Introduction

SELECTIVE Epitaxial Growth (SEG) of silicon has been identified as a key technology for future VLSI/ULSI processes [1], [2]. SEG, ELO (Epitaxial Lateral Overgrowth), and CLSEG (Confined Lateral Selective Epitaxial Growth) have been used to fabricate many novel bipolar, CMOS, and BiCMOS devices [1]–[4]. These selective growth techniques have been used to grow high quality silicon to make active device regions or to grow poly-silicon for applications where material quality is not important such as contacts, trench fills [5], etc. When high quality silicon is desired, the characteristics, texture, and morphology of the seed-hole surface has to be excellent. In most applications of silicon SEG, the seed-hole is etched through an oxide, using a reactive ion etch (RIE). The RIE step leaves damage, due to the ion-bombardment and residual polymers. It is essential that the high surface quality be restored prior to the SEG process. This is conventionally achieved by growing a thin sacrificial oxide layer. The high temperature of oxidation eliminates any polymers left behind and also consumes the damaged silicon region. The grown oxide is removed using a wet-etch prior to selective epitaxial growth. Drawbacks of this oxidation are additional thermal diffusion and the need for a wet etch which affects the dimensional control of etch windows.

In this letter, we present a process flow which eliminates the need of the sacrificial oxidation. After the seed-hole oxide was etched in a $CHF_3/C_2F_6$ RIE, a short, low power $C_2F_6$ etch was performed. These wafers were compared with two other process flows: 1) wafers in which the seed-hole was wet-etched, 2) wafers where oxide was etched in $CHF_3/C_2F_6$ RIE, and 3) wafers where a reoxidation step was performed after the dry-etch. $N$-type SEG silicon was grown in $P$-type $\langle 100 \rangle$ substrates in all wafers and the resulting diode formed at the substrate/SEG interface was used to evaluate the quality of the interface and hence the quality of the silicon surface prior to SEG. The diodes formed on wafers with the low power $C_2F_6$ etch and no sacrificial oxidation exhibited ideality factors which were the same as the diodes resulting from the wet-etched seedhole and the reoxidized seed-hole diodes. The new process flow provides a very simple and cost-effective way to eliminate RIE damage prior to SEG growth because the dry low power $C_2F_6$ etch can be done in the same etch reactor in which the seed-hole oxide etch is performed. In addition, the reoxidation step is eliminated, hence, reducing the number of process steps.

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The authors are with Analog Process Technology Development, National Semiconductors, Santa Clara, CA 95051 USA.

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## II. Diode Fabrication

An *np* junction diode was used as the device to characterize the surface treatment used prior to selective epitaxial growth. 1.0 $\mu$m of thermal oxide was grown on $\mathbf{P}\langle 100 \rangle$ substrates with resistivity of 12–15 $\Omega$-cm. Various processes were then used to open the seed-hole prior to selective epitaxial growth of silicon as described in the following.

*Process 1:* This process was used as the control. The 1.0 $\mu$m of thermal oxide was wet-etched using BHF solution with a photoresist mask. The photoresist mask was then stripped using piranha (1:1 $H_2O_2$:$H_2SO_4$) clean.

*Process 2:* The 1.0 $\mu$m of thermal oxide was etched using a $CHF_3/C_2F_6$ (114 sccm: 38 sccm) RIE in a LAM 384 Triode etcher at 130 mT and 450 watts with the bias applied to the wafer electrode. The etch produced vertical sidewall and had a selectivity of 8:1 (oxide:silicon). The etch had an automatic endpoint with a 20% over-etch. This insured the complete etching of the oxide to expose the silicon surface across the entire wafer. The photoresist mask was stripped using piranha (1:1 $H_2O_2$:$H_2SO_4$) clean.

*Process 3:* In this process, the oxide was etched in the same manner as Process 2. After the oxide was etched, the photoresist mask was stripped using piranha (1:1 $H_2O_2$:$H_2SO_4$) clean. The wafer was then oxidized at 1050°C in dry $O_2$ to result in 500 Å of oxide. The oxide was then wet-etched using a BHF solution prior to the selective epitaxial growth.

*Process 4:* After the masking oxide was etched as described in Process 2 in the LAM 384T etcher, another step was added to the etch recipe. A 10 second etch using $C_2F_6$ plasma at 150 watts and 130 mT was used. The purpose of this etch is to remove the RIE damage and residual polymer by removing 50–100 Å of the silicon surface. The photoresist mask was then removed using a piranha clean followed by a short BHF dip.

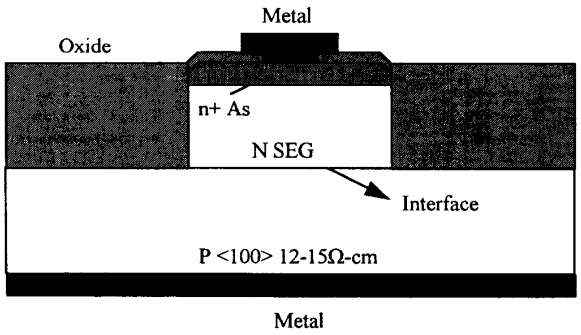


Fig. 1. Cross section for the diodes of processes 2–4 showing RIE sidewall and the diode formed at the $N$ SEG/$P$ substrate junction. The diode of process 1 had a sloped sidewall due to the wet-etching of the seed-hole oxide.

All wafers were then cleaned in a megasonic cleaner in $H_2O_2$:$NH_4OH$ solution. The wafers were then placed in a Applied Materials 7800 barrel reactor. A two minute $H_2$ bake and a 30 second HCl etch, both at 980°C, were used prior to the growth. SEG was then grown from the silicon seed-holes at 980°C, 40 torr at a growth rate of 0.17 $\mu$m/min to result in 1 $\mu$m of growth. The SEG was arsenic doped at a concentration of $7\times10^{15}$ cm$^{-3}$. After the SEG, arsenic was implanted in the $n$-type silicon at 60 keV with a dose of $5\times10^{15}$ cm$^{-3}$. LTO was deposited and densified at 1050°C for 15 minutes which also activated the implant. Contacts were opened and the wafers were metalized. The cross-section of the fabricated diodes is shown in Fig. 1.

## III. Results and Discussion

Fig. 2 shows the forward biased I-V plots and ideality factors for the four diodes. The diode was circular with an area of about 5000 $\mu$m$^{-2}$. Table I lists the measured device parameters. The control diode of Process 1 exhibited a very smooth surface morphology after the SEG and average ideality factor of 1.28. The fact that the ideality factor is higher than 1.0 can be explained by the sidewall defects generated due to thermal stress during the cool-down period after the SEG growth [6]. The dry etched diode of Process 2 resulted in a rough surface after SEG when observed through nomarski microscope and the worst ideality factor of 1.79 indicating excessive recombination in the forward biased depletion region due to surface damage. The excess current can be attributed to the presence of defects at the substrate-SEG interface resulting from the RIE of the oxide. SUPREM-3 simulations show that the diode junction is about 400 A below the SEG/substrate interface due to the diffusion of arsenic from the SEG into the substrate. The forward biased depletion width at 0.5 V can be calculated to be about 600 A. Thus any defects at the SEG/substrate interface will be manifested in the diode I-V characteristics. It should be noted that the HCl etch prior to SEG was not effective, most probably because the residual polymer does not get etched. When the silicon surface was oxidized, the damaged region was consumed and the resulting SEG diodes quality was restored to ideality factors of 1.3.

TABLE I
List of Measured Electrical Parameters on the Four Processes. The Data is Averaged over 12 Devices.

| Sample Type | Ideality Factor | Leakage @ -10V | BV @ 10μA |
|---|---|---|---|
| Process 1 | 1.28 | 0.31pA/μm$^2$ | 92V |
| Process 2 | 1.79 | 2.2pA/μm$^2$ | 81V |
| Process 3 | 1.30 | 0.62pA/μm$^2$ | 86V |
| Process 4 | 1.22 | 0.31pA/μm$^2$ | 81V |

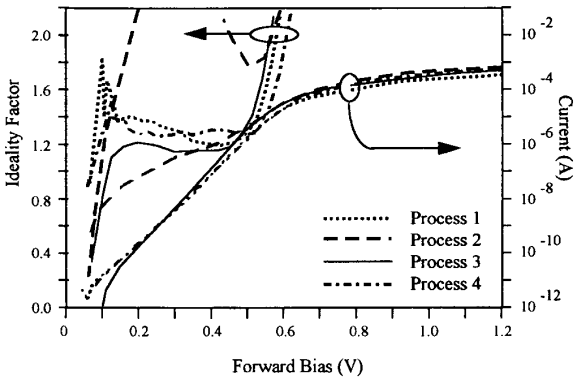


Fig. 2. Typical forward bias I-V characteristics and ideality factors of the diodes using the 4 different processes. As shown, the ideality factor is highest for the RIE seed-hole diode.

Most importantly, the diode of Process 4 resulted in electrical characteristics nearly the same as that of Processes 1 and 3. The low power $C_2F_6$ etched the residual polymer from the oxide etch and also removed some of the damaged silicon. Since the $C_2F_6$ etch was performed in the same reactor as the oxide etch, the process was simple and cost-effective. The reverse leakage currents showed trends similar to the ideality factors. Except for the fact that the Process 2 diodes exhibited soft breakdown, the breakdown voltages measured at 10 $\mu$A were relatively independent of the surface treatment.

## IV. Conclusion

The purpose of this letter was to report the results of a simple and manufacturable process to produce high quality silicon surface prior to selective epitaxial growth. A low power $C_2F_6$ etch was used after the oxide etch in the same reactor to remove residual polymers and RIE damage. $N$-type SEG was grown on $P$-type substrate to form diodes and evaluate the interface quality and hence the surface preparation prior to SEG. It was shown that the diodes with the *in-situ* $C_2F_6$ etch resulted in excellent surface quality, thus eliminating the need for the conventional sacrificial oxidation step.

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